(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 213 641**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 86112327.1

(51) Int. Cl.⁴: H04L 25/14 , H04J 3/06

(22) Date of filing: 04.09.86

(30) Priority: 04.09.85 JP 195623/85

(43) Date of publication of application:
11.03.87 Bulletin 87/11

(84) Designated Contracting States:
DE FR GB

(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Sakata, Takashi
2-1-2, Fujigaoka Midori-ku
Yokohama-shi Kanagawa 227(JP)
Inventor: Hanabata, Toshio
1-3-1-523, Aobadai Midori-ku
Yokohama-shi Kanagawa 227(JP)
Inventor: Fujimoto, Naonobu
2264, Kizuki Ise-cho Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)
Inventor: Murase, Tetsuro
Tokan-manshion Yamato 303 95-1,
Kashiwaba
Naka-ku Yokohama-shi Kanagawa 231(JP)
Inventor: Ikawa, Fumihiro
2-13-13, Edaklta Midori-ku
Yokohama-shi Kanagawa 227(JP)

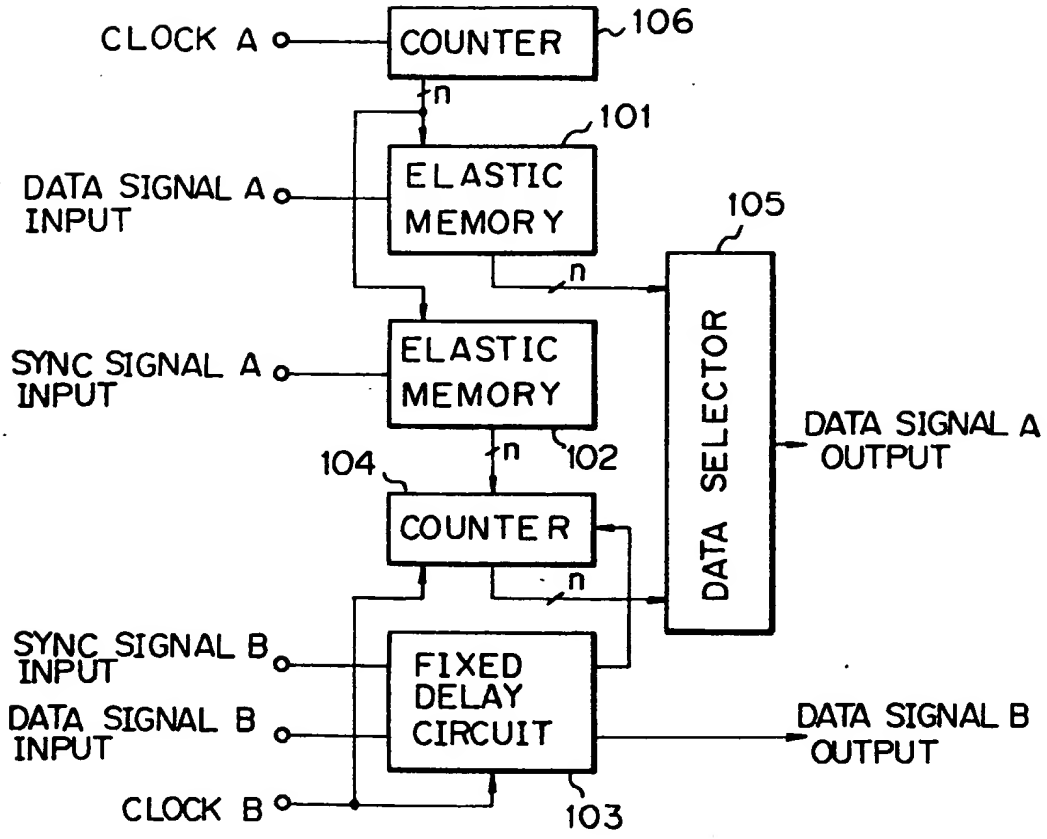
(74) Representative: Lehn, Werner, Dipl.-Ing. et al
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4 (Sternhaus)
D-8000 München 81(DE)

(54) Delay time adjusting method, circuit, and system.

(57) In a delay time adjusting circuit, a transmitter device divides original data into a first data signal and a second data signal and sends the first data signal and the second data signal via different transmission paths to a receiving device, and the receiving device mixes the first data signal and the second data signal so as to reproduce the original data. In the receiving device, the first data signal is written in first elastic memory (101) and is operated in response to a clock of the first data signal, the second data signal is delayed and corresponding bits of the first elastic memory (101) are sequentially read out in response to an output of a ring counter (104) having the same number of bits as that of the first elastic memory (101) and operated in response to a clock of the second signal, and to which the position of the first data signal in the first elastic memory (101) is loaded in response to the delayed second data signal.

EP 0 213 641 A2

Fig. 4


CLOCK A
COUNTER
106
n
101
DATA SIGNAL A INPUT
ELASTIC MEMORY
105
n
SYNC SIGNAL A INPUT
ELASTIC MEMORY
DATA SELECTOR
DATA SIGNAL A OUTPUT
n
102
104
COUNTER
n
SYNC SIGNAL B INPUT
FIXED DELAY CIRCUIT
DATA SIGNAL B INPUT
DATA SIGNAL B OUTPUT
CLOCK B
103

DELAY TIME ADJUSTING METHOD, CIRCUIT, AND SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a signal transmission system and, more particularly, to a delay time compensation circuit for absorbing a difference between delay times of two signals, which are divisionally transmitted, using an elastic memory.

Description of the Related Art

The frequency band of a television signal in an RAL system is 0 ~ 5 MHz. When this signal is sampled by 13 MHz in accordance with a sampling theorem and is expressed by 8 bits per one sampling value, it becomes 104 Mbps.

Usually, this 104 Mbps signal is not sent in its original form, but 68 Mbps is used by a band compression such as DPCM, etc.

However, according to CCITT recommendation a bierarchy of the transmission path for transmitting this signal should be 2 MHz, 8 MHz, 34 MHz, and 140 MHz.

As seen from the above, the speed at which the 68 Mbps signal in its original form can be transmitted is only 140 MHz, and this is uneconomical because the whole transmission capacity is not used.

Therefore, the technique by which the 68 Mpps is divided into two signals and is transmitted as two 34 Mbps signals is considered in the present invention.

In terms of the capacity of the transmission path, a single high-speed signal must often be transmitted after being divided into a plurality of low-speed signals, and the low-speed signals must be mixed to obtain the original high-speed signal again at the reception side. In this case, in order to appropriately receive the two signals at the reception side, the propagation delay times of the two signals should be equal. In practice, however, a difference in propaga tion delay times occurs, due to various causes.

The major causes of the difference in propagation delay times include a difference between signal propagation times inherent to the transmission paths.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an effective means for absorbing the difference in delay times which occurs in the transmission path.

The above mentioned object can be achieved by providing a delay time adjusting method in which a transmitter device divides original data into a first data signal and a second data signal and sends the first data signal and the second data signal via different transmission paths to a receiving device, and the receiving device mixes the first data signal and said second data signal so as to reproduce the original data. The present invention is characterized in that, in the receiving device, the first data signal and a sync signal synchronous therewith are simultaneously written in first and second elastic memories, which have the same bit length and are operated in response to a clock of the first data signal, the second data signal and a sync signal synchronous therewith are delayed by the same time period, and corresponding bits of the first elastic memory are sequentially read out in response to an output of a ring counter, which has the same number of bits as that of the first and second elastic memories and is operated in response to a clock of the second signal, and to which the position of the first sync signal in the second elastic memory is loaded in response to the delayed second sync signal.

Further, the above mentioned object can be achieved by providing a delay time adjusting circuit in a signal transmission system in which a high-speed data signal is divided into two low-speed data signals, the low-speed signals are transmitted through different transmission paths, and after a difference in delay times between the two signals is absorbed at a reception side, the low-speed signals are mixed again. This aspect is characterized in that a first signal and a sync signal synchronous therewith are simultaneously written in first and second elastic memories which have the same bit length and are operated in response to a clock of the first signal; a second signal and a sync signal synchronous therewith are delayed by the same time period by a fixed delay circuit; the position of the first sync signal in the second elastic memory is loaded, in response to the delayed second sync signal, in a counter, which has the same number of bits as that of the first and second elastic memories and is operated in response to a clock of the second signal; and corresponding bits of the first elastic memory are sequentially read out through a data selector in

response to the output from the counter, thereby obtaining a first signal output, from which the difference in the delay times with respect to the second signal is absorbed.

Still further, the above mentioned object can be achieved by providing a delay time adjusting system in which the phases of first and second inputs of third multiplexed data having a phase difference of ±D bits, and in which the first input consisting of a bipolar signal is converted to a unipolar signal by a first bipolar/unipolar converter, and a high density bipolar (HDB3) code is decoded by a first HDB3 decoder, thus producing a 34 MHz clock signal as well as a 34-Mb/sec data signal, a first demultiplexer demultiplexes these signals and produces eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal, the eight data signals and the frame signal are delayed through nine D/8-bit delay circuits in a fixed delay circuit, and a first data signal is output as output data DATA OUTl, and a second data input similarly passes through a second bipolar/unipolar converter, a second HDB3 decoder, and a second demultiplexer, thus producing eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal, the eight data signals and the frame signal are input to a variable delay circuit, and are delayed through nine D/4-bit delay circuits. This aspect is characterized in that the variable delay circuit receives the 4 MHz clock signal from the second demultiplexer as a write clock, the 4 MHz clock signal from the first demultiplexer as a read clock, and the frame signal passing through the fixed delay circuit as a delay sync signal, thereby producing output data DATA OUT2 which is phase-locked with the output data DATA OUTl.

Further feature and advantages of the present invention will be apparent from the ensuring description with reference to the accompanying drawings to which, however, the scope of the invention is in no way limited.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure l is a block diagram of a signal transmission system to which the circuit of the present invention is applied;

Fig. 2 is a timing chart showing the data which flows in the system shown in Fig. l;

Fig. 3 is a timing chart explaining the principle of the present invention;

Fig. 4 is a block diagram of the circuit of the present invention;

Fig. 5 is a block diagram of one embodiment of the circuit according to the present invention;

Fig. 6 is a timing chart showing the respective signals in the embodiment shown in Fig. 5; and

Fig. 7 is a block diagram of a signal transmission system to which the circuit of the present invention is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure l is a block diagram of a signal transmission system to which the circuit of the present invention is applied; and Fig. 2 is a timing chart showing the data which flows in the system shown in Fig. l.

In Fig. l, a transmitter device l modulates a PAL video signal to a DPCM (differential pulse code modulation) form to prepare a 68-Mb/sec signal, and the 68-Md/sec signal is divided into two low-speed signals A and B through a distribution device 2. The signals A and B are transmitted through transmission paths 3 and 4 having a transmission rate of 34.368 Mb/sec rated by the CCITT recommendation, and are mixed by a mixing device 5 to reproduce the 68-Mb/sec signal. The reproduced signal is then received by a receiver device 6.

In Fig. 2, (a) is an original data (DPCM signal), (b) is transmitted data having substantially the same phase and transmitted on the transmission lines A and B, and (c) is received data. In this case, a difference of propagation time occurs between the received data A and B.

Figure 3 is a timing chart showing a principle of adjusting the difference of the propagation time between the data A and the data B mentioned above.

In Fig. 3, (a) shows a data signal A, (b), (c) and (d) are contents of elastic memories storing the content of the data, which is divided into three portions and delayed by one bit of data. In Fig. 3, (e), (g), (i) are the data signal B, wherein (e) is in phase with the data signal A, (g) is advanced to the data signal B by l.5 bits, and (i) is delay from the data signal B by l.5 bits. In the present invention, the data signal (e), (g) and (i) are delayed by the same bit as (f), (h), (j) in Fig. 3. As shown in Fig. 3, the delayed data (f), (h) and (i) are positioned in the range where the corresponding data are stored in the data (b), (c) and (d). For example, data "l" in the data signal B are positioned in the range of data "l" in the data signal (b) regardless of when the signal data B is advanced or delayed as shown in (h) or (j).

Figure 4 shows an arrangement based on the principle of the present invention.

Reference numerals l0l and l02 denote first and second elastic memories, respectively, and l06, a counter. The first and second elastic memories l0l, l02 simultaneously receive a first data signal A -

(shown in Fig. 3 (a)) and a sync signal A (shown in Fig. 3 (a')) synchronous therewith, which have the same bit length, and are operated in response to an output from the counter 106 for counting clocks A synchronous with the data signal A. Then the data (b), (c), (d) shown in Fig. 3 are read out from the elastic memory 101.

Reference numeral 103 denotes a fixed delay circuit, which delays a second data signal B shown in (e), (g), (i) of Fig. 3 and a sync signal B (shown in Fig. 3 (e'), (g'), (i')) synchronous therewith by the same numter of bits.

Reference numeral 104 denotes a counter, which has the same number of bits as that of the first and second elastic memories 101 and 102 and is operated in response to the clocks B synchronous with the second data signal B. In addition, the counter 104 loads the position of the first sync signal A shown in Fig. 3 (a') in the elastic memory 102 in response to the delayed second sync signal B (shown in Fig. 3 (f'), (h'), (j')).

Reference numeral 105 denotes a data selector for sequentially reading out the corresponding data signal A (shown in Fig. 3 (b), (c), (d)) from the first elastic memory 101 in response to the output from the counter 104.

Where it is assumed that the data signals A and B are received in phase, in advance phase (for example, 1.5 bit) or delayed phase (for example 1.5 bit).

The data signal A is divided by the elastic memory 101 into n (for example three) phase signals and accordingly, each phase signal becomes n bit (for example, 3 bits) in width.

At the same time, the data singal B and the sync signal B are delayed n/2 bit (in this example 1.5 bit) by the fixed delay circuit 103. (Fig. 3 (f), (h), (j))

Here, the data selector 105 reads, in order, the output of the elastic memory 101 in accordance with the clock from the counter 104, and the phase of the clock of the counter 104 coincides with the phase of the sync signal B, then the phase of the data signal A from the data selector 105 coincides with the phase of the data signal B from the fixed delay circuit 103.

Figure 5 shows one embodiment of the present invention, in Fig. 5, reference numeral 11 denotes a 3-bit ring counter; and 12, a NAND gate. Reference numerals 13, 14, and 15 denote flip-flops (to be referred to as F•Fs hereinafter), which constitute a 3-bit memory cell, that is, the elastic memory cell 101 shown in Fig. 4. Reference numeral 18 denotes a data selector corresponding to 105 in Fig. 4. Reference numerals 21, 22, and 23 denote flip-flops (to be referred to as F•Fs hereinafter), which constitute a 3-bit memory cell that is, the elastic memory cell 102 in Fig. 5. Reference numeral 24 - (corresponds to 103 in Fig. 4) denotes a fixed delay circuit. Figure 5 exemplifies a case wherein one data input B of two data inputs A and B is constantly delayed by 1.5 bits by the fixed delay circuit 24, and the other data input A is variably delayed through a 3-bit elastic memory. The sync signals A and B are signals indicating the positions of the phases of the data inputs A and B at the transmission side.

Figure 6 shows the respective signals in the emtodiment shown in Fig. 5. In Fig. 6 ⓐ indicates a write clock A input; ⓑ , ⓒ , and ⓓ , Q_1 , Q_2 , and Q_3 outputs of the 3-bit ring counter 11, respectively; ⓔ , a data A input; ⓕ , ⓖ , and ⓗ , Q outputs of the F•F 13 the F•F 14, and the F•F 15, respectively; i , a sync signal B input; ⓙ , ⓚ , and ⓛ , Q outputs of the F•F 21, the F•F 22, and the F•F 23, respectively; ⓜ , a sync signal B input, ⓝ , an output of the fixed delay circuit 24, ⓞ , ⓟ , and ⓠ , Q_1, Q_2 and Q_3 outputs of the 3-bit ring counter 16, respectively; ⓡ , ⓐ data B' output of the fixed delay circuit 24, and s , a data A' output of the data selector 18.

The ring counter 11 generates three phase clock outputs ⓑ , ⓒ , and ⓓ which sequentially go to "1" level at every leading edge of the write clock A synchronous with the data A input indicated by ⓐ from the output terminals Q, , Q_2 , and Q_3 thereof. The F•F 13, and F•F 14, and F•F 15 constituting the memory cell respectively receive the parallel data A inputs (1, 2, 3, ...) indicated by ⓔ at their data terminals D and also receive the clocks ⓑ , ⓒ , and ⓓ at their clock terminals CK. The F•F 13, F•F 14, and F•F 15 retrieve the data A inputs in response to the trailing edges of the clocks ⓑ , ⓒ , and ⓓ , thus generating the outputs f (1, 4, ...), g (2, 5, ...) and h (3, 6, ...) from their Q outputs.

The F•F 21, F•F 22, and F•F 23 respectively receive the parallel sync signal A input indicated by ⓘ at their data terminals D and the clocks ⓑ , ⓒ , and ⓓ at their clock terminals CK, and retrieve the sync signal A in response to the leading edges thereof. The sync signal A is synchronous with a signal (i) in the data A input. The F•F 21 loads a "1" in response to the trailing edge of the clock ⓑ , and holds a "1" at its output ⓙ during a 3-bit interval until the clock ⓒ trails again. On the other hand, the outputs ⓚ and ⓛ are at "0" level.

The data B input and the sync signal B input indicated by ⓜ are delayed by 1.5 bits by the fixed delay circuit 24, thus producing the data B output and the sync signal output ⓝ . The

3-bit ring counter I6 receives the sync signal output ⓝ at its load terminal LOAD. When the signal ⓝ is at "I"-level, the counter I6 loads the values of the outputs ⓙ , ⓚ , and ⓔ applied to its data terminals D_1 , D_2 , and D_3 in response to the leading edge of the read clock B input, thereby producing the outputs ⓞ , ⓟ , and ⓠ , respectively. In this case, the output ⓞ , is at "I" level, and the outputs ⓟ and ⓠ are at "0" level.

When the output ⓞ goes to "I" level, the data selector I8 selects and outputs the data ⓕ of the corresponding F•F I3, thereby producing data of (I) from the data A' output. The 3-bit ring counter I6 receives the read clock B input at its clock terminal CK, and generates the outputs ⓞ , ⓟ , and ⓠ from the terminals Q_1 , Q_2 and Q_3 which subsequentially go to "1" level, respectively. In response to the outputs ⓞ , ⓟ , and ⓠ , the data selector I8 sequentially selects and outputs the data ⓕ , ⓖ , and ⓗ . Thus, data of (2), (3), (4), ... are sequentially selected and are output to the data A output indicated by ⓢ .

In this manner, the data A is phase-locked with the sync signal B (ⓝ) passing through the fixed delay circuit 24 and is output to the output ⓢ via the data selector I8, thereby adjusting the phase difference between the data A and B.

According to the embodiment shown in Fig. 5, when the data A input has the phase difference falling within the range of ±I.5 bits compared to the data B input, this difference can be adjusted to lock their phases.

Referring to Fig. 6B, ⓐ indicates a case wherein the date B input advances from the data A input by I.5 bits, and ⓑ indicates a case wherein the data B input is delayed from the data B input by I.5 bits. In this case, since the sync signal B (ⓝ) passing through the fixed delay circuit 24 also advances or is delayed by I.5 bits, the data A output indicated by ⓢ also advances or is delayed by the same numter of bits. Therefore, the phase adjustment with respect to the data A output can be similarly performed.

Figure 7 shows a practical application of the method of the present invention to an apparatus. Figure 7 exemplifies a case wherein the phases of inputs I and 2 of third multiplexed data D3, which have the phase difference of ±D bits, are adjusted. A first input D3 INI consisting of a bipolar signal is converted to a unipolar signal by a bipolar/unipolar converter (B/U) 3I, and a high density bipolar - (HDB3) code is decoded by an HDB3 decoder - (HDB/3/U) 32, thus producing a 34 MHz clock signal as well as a 34-Mb/sec data signal. A demultiplexer (DMUX) 33 demultiplexes these signals and produces eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal. The eight data signals and the frame signal are delayed through nine D/8-bit delay circuits in a fixed delay circuit 34, and the data signal is output as output data DATA OUTI.

Meanwhile, a second data input D3 IN2 similarly passes through a bipolar/unipolar converter - (B/U) 35, and HDB3 decoder (HDB3/U) 36, and a demultiplexer (DMUX) 37, thus producing eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal. The eight data signals and the frame signal are input to a variable delay circuit 38, and are delayed through nine D/4-bit delay circuits. The variable delay circuit 38 as the main feature of the present invention uses the 4 MHz clock signal from the DMUX 37 as a write clock, the 4 MHz clock signal from the DMUX 33 as a read clock, and the frame signal passing through the fixed delay circuit 34 as a delayed sync signal, and is operated in the same manner as in the emtodiment shown in Fig. 5, thereby producing output data DATA OUT2 which is phase-locked with the output data DATA OUTI.

According to the signal transmission method of the present invention as described above, one signal is applied to an elastic memory to read out data therefrom and obtain an output in response to a ring counter output which is stepped by the number of bits corresponding to a difference between delay times of the sync signals of two signals, and the other signal is constantly delayed by a given number of bits. Therefore, even if one signal is either advanced or delayed from the other signal, any difference in the delay times can be absorbed.

Claims

I. A delay time adjusting method in which a transmitter device divides original data into a first data signal and a second data signal and sends said first data signal and said second data signal via different transmission paths to a receiving device, and said receiving device mixes said first data signal and said second data signal so as to reproduce said original data, characterized in that in said receiving device, said first data signal is written in first elastic memory and is operated in response to a clock of said first data signal, said second data signal is delayed and corresponding bits of said first elastic memory are sequentially read out in response to an output of a ring counter having the same number of bits as that of the first elastic memory and operated in response to a clock of the second signal, and to which the position of the first data signal in the first elastic memory is loaded in response to the delayed second data signal.

2. A delay time adjusting circuit in a signal transmission system in which a high-speed data signal is divided into two low-speed data signals, the low-speed signals are transmitted through different transmission paths, and after a difference in delay times between the two signals is absorbed at a reception side, the low-speed signals are mixed again, characterized in that

a first signal and a sync signal synchronous therewith are simultaneously written in first and second elastic memories (I01, I02) having the same bit length and are operated in response to a clock of the first signal;

a second signal and a sync signal synchronous therewith are delayed by the same time period by a fixed delay circuit (I03);

the position of the first sync signal in said second elastic memory is loaded, in response to the delayed second sync signal, in a counter (I04) having the same number of bits as that of said first and second elastic memories and operated in response to a clock of the second signal; and

corresponding bits of said first elastic memory are sequentially read out through a data selector (I05) in response to the output from said counter, thereby obtaining a first signal output, from which the difference in the delay times with respect to the second signal is absorbed.

3. A delay time adjusting system in which the phases of first and second inputs of third multiplexed data having a phase difference of ±B bits and in which said first input consisting of a bipolar signal is converted to a unipolar signal by a first bipolar/unipolar converter (31), and a high density bipolar (HDB3) code is decoded by a first HDB3 decoder (32), thus producing a 34 MHz clock signal as well as a 34-Mb/sec data signal, a first demultiplexer (33) demultiplexes these signals and produces eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal said eight data signals and said frame signal are delayed through nine D/8-bit delay circuits in a fixed delay circuit (34), and a first data signal is output as output data DATA OUT1, and a second data input similarly passes through a second bipolar/unipolar converter, a second HDB3 decoder (36), and a second demultiplexer (37), thus producing eight 4-Mb/sec data signals, a 4 MHz clock signal, and a frame signal, said eight data signals and said frame signal are input to a variable delay circuit (38), and are delayed through nine D/4-bit delay circuits, characterized in that said variable delay circuit receives the 4 MHz clock signal from said second demultiplexer (37) as a write clock, the 4 MHz clock signal from said first demultiplexer (33) as a read clock, and the frame signal passing through said fixed delay circuit (34) as a delayed sync signal, thereby producing output data DATA OUT2 which is phase-locked with the output data DATA OUT1.

Fig. 1

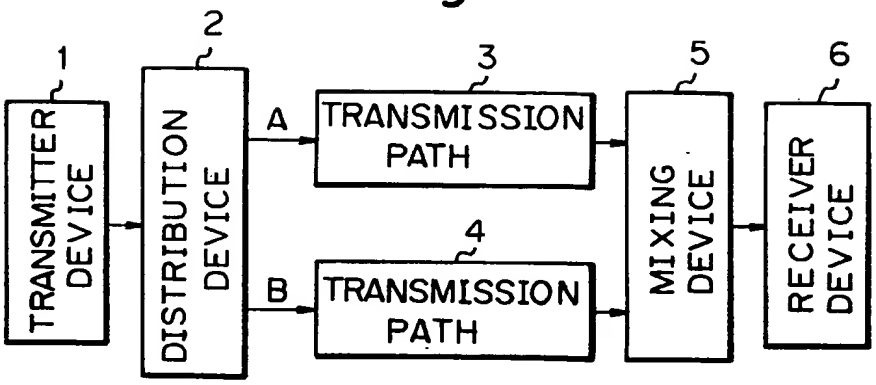

1
2
3
5
6
TRANSMITTER DEVICE
DISTRIBUTION DEVICE
A
TRANSMISSION PATH
4
B
TRANSMISSION PATH
MIXING DEVICE
RECEIVER DEVICE

Fig. 4

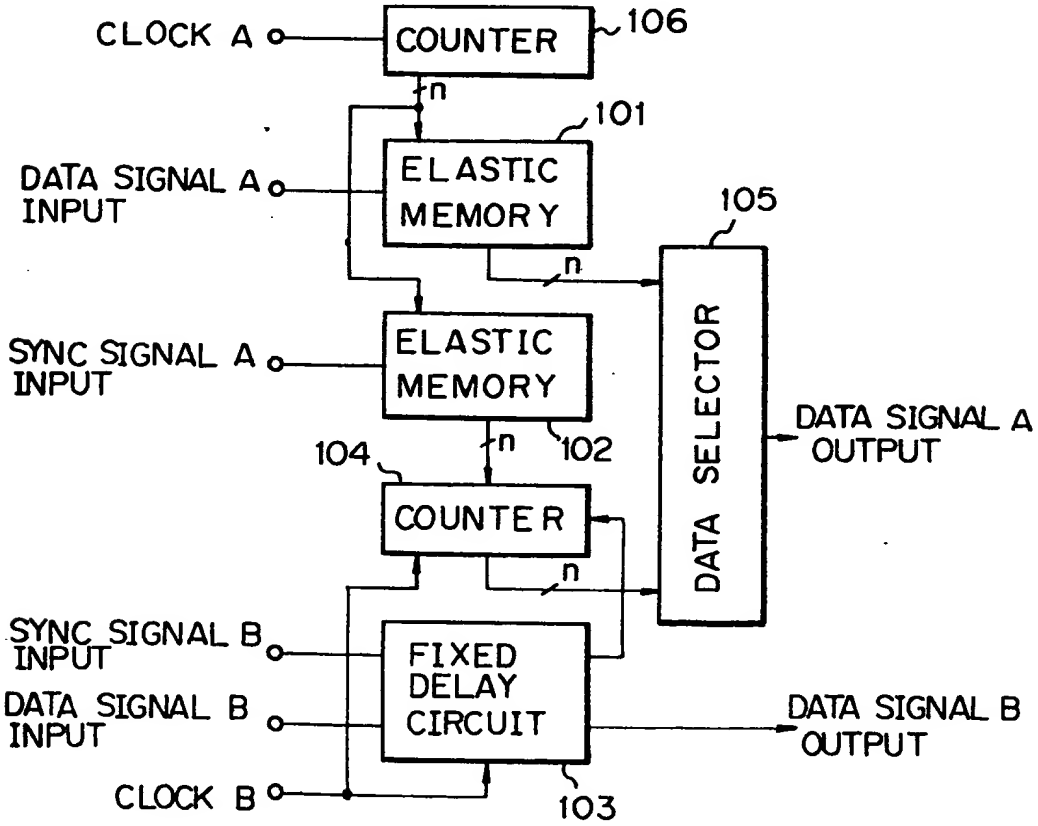

CLOCK A
COUNTER
106
n
101
DATA SIGNAL A INPUT
ELASTIC MEMORY
105
n
SYNC SIGNAL A INPUT
ELASTIC MEMORY
DATA SELECTOR
DATA SIGNAL A OUTPUT
n
102
104
COUNTER
n
SYNC SIGNAL B INPUT
FIXED DELAY CIRCUIT
DATA SIGNAL B INPUT
DATA SIGNAL B OUTPUT
CLOCK B
103

Fig. 2

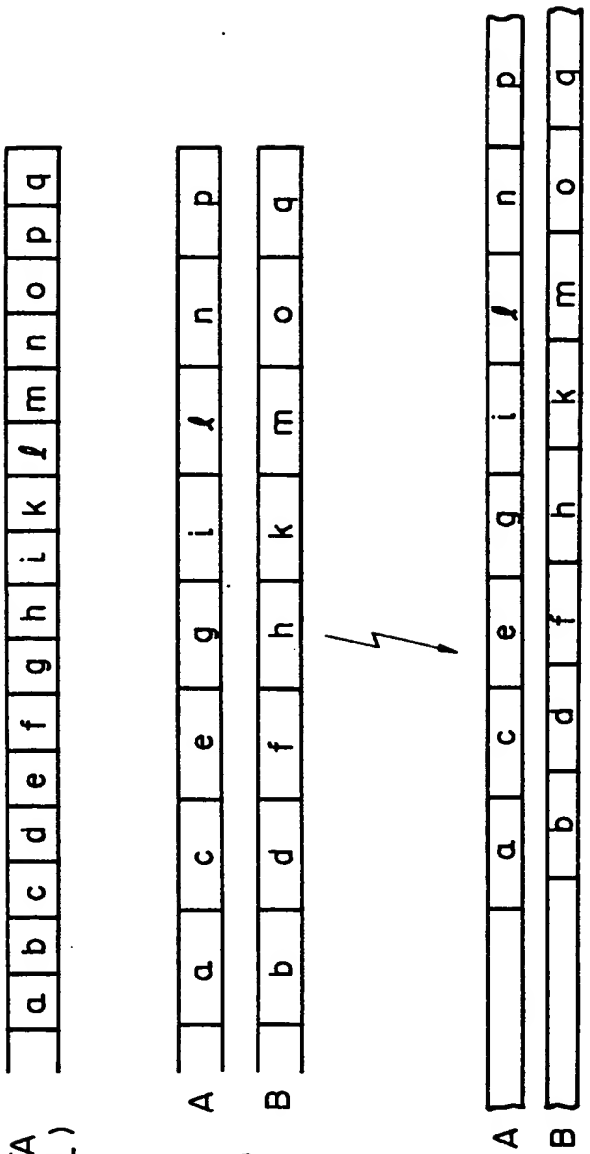

(a) ORIGINAL DATA (DPCM SIGNAL)
a b c d e f g h i k l m n o p q
(b) TRANSMITTING DATA
A
a c e g i l n p
B
b d f h k m o q
(c) RECEIVED DATA
A
a c e g i l n p
B
b d f h k m o q

Fig. 3

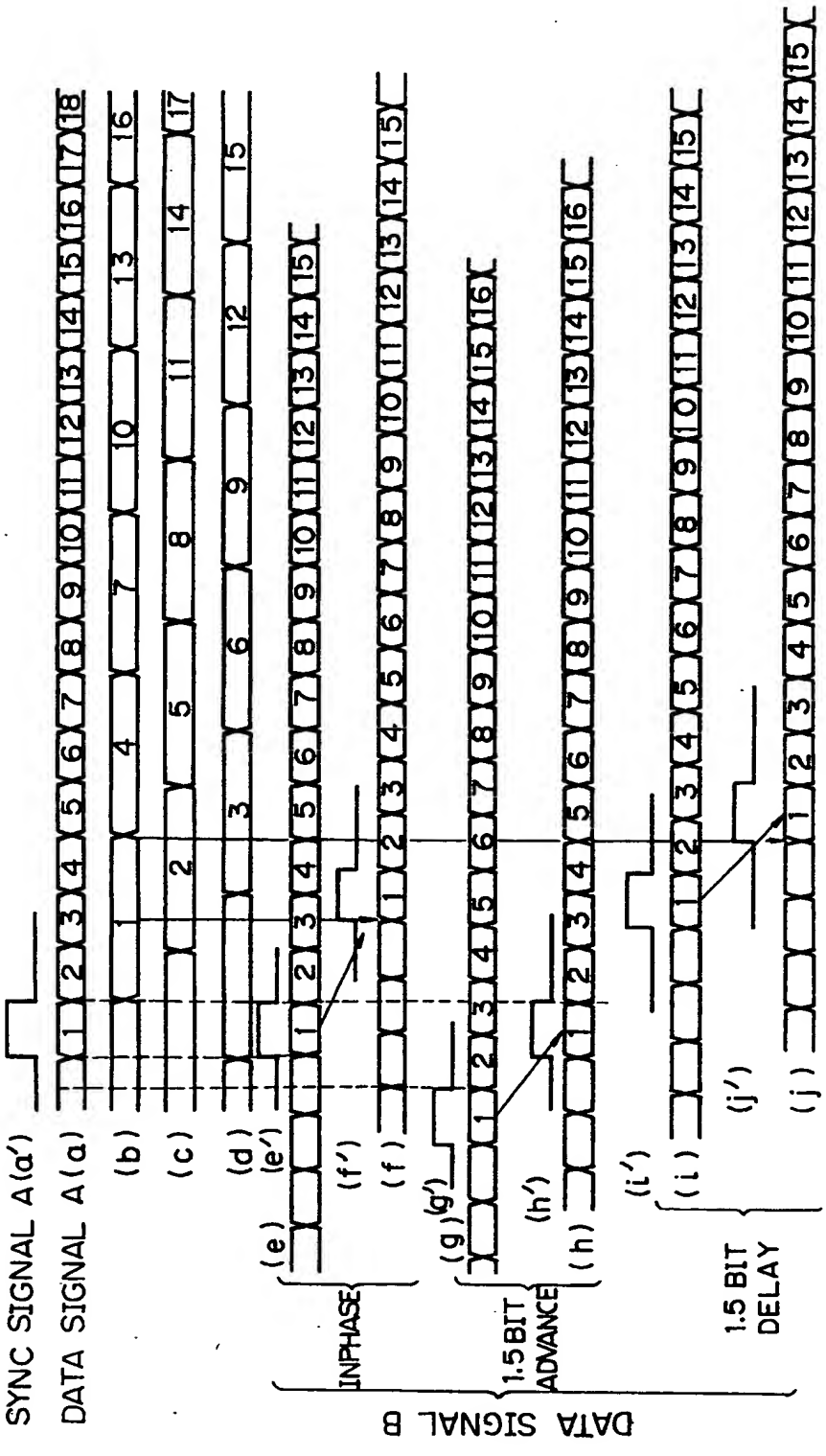

SYNC SIGNAL A(a')
DATA SIGNAL A(a)
(b)
(c)
(d)
(e')
(e)
(f')
(f)
(g')
(g)
(h')
(h)
(i')
(i)
(j')
(j)
INPHASE
1.5 BIT ADVANCE
1.5 BIT DELAY
DATA SIGNAL B

Fig. 5

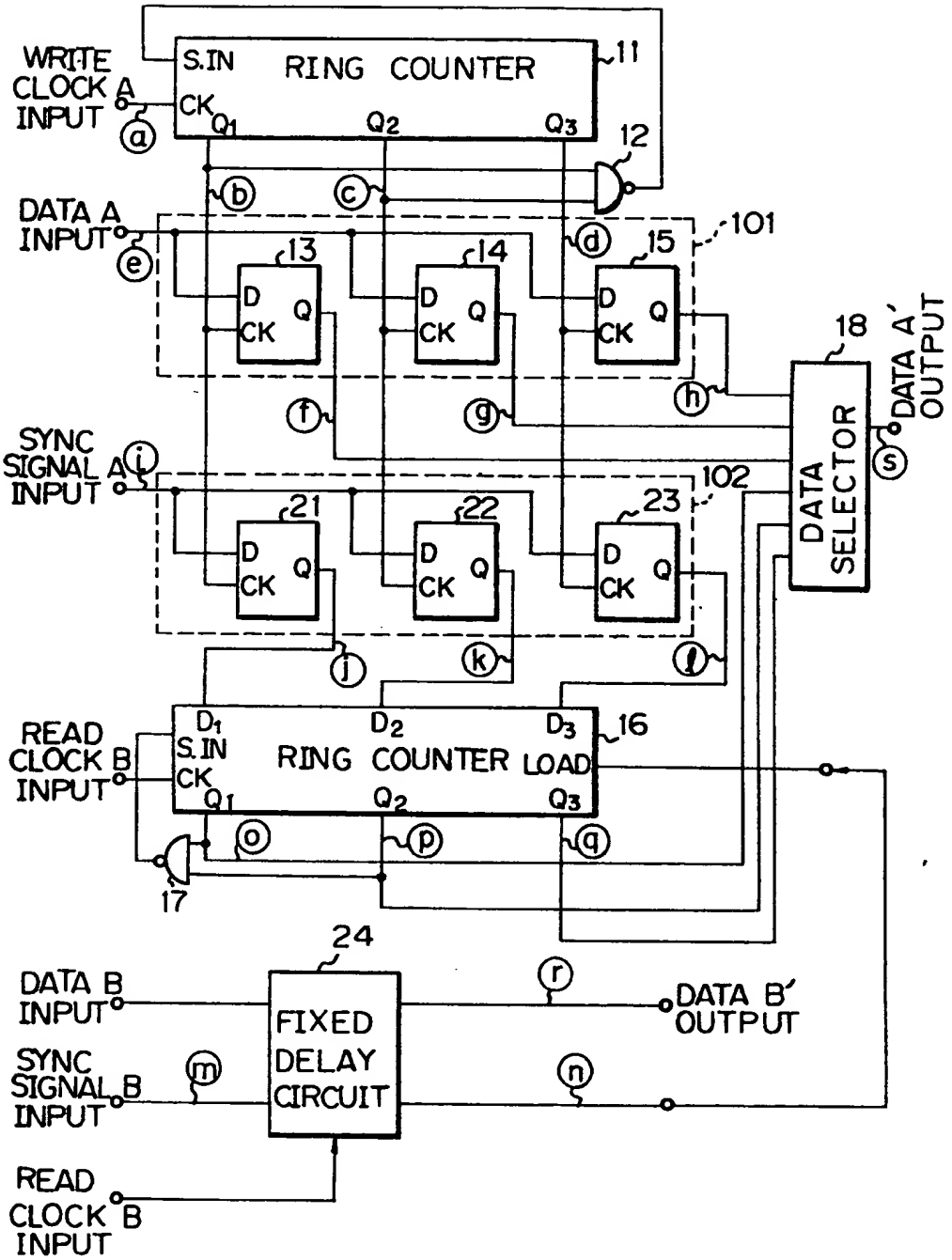

WRITE CLOCK A INPUT
S.IN
CK
RING COUNTER
Q1
Q2
Q3
11
12
DATA A INPUT
101
13
14
15
D
CK
Q
18
DATA A' OUTPUT
DATA SELECTOR
SYNC SIGNAL A INPUT
102
21
22
23
READ CLOCK B INPUT
D1
D2
D3
LOAD
16
17
24
DATA B INPUT
FIXED DELAY CIRCUIT
DATA B' OUTPUT
SYNC SIGNAL B INPUT
READ CLOCK B INPUT

Fig. 6A

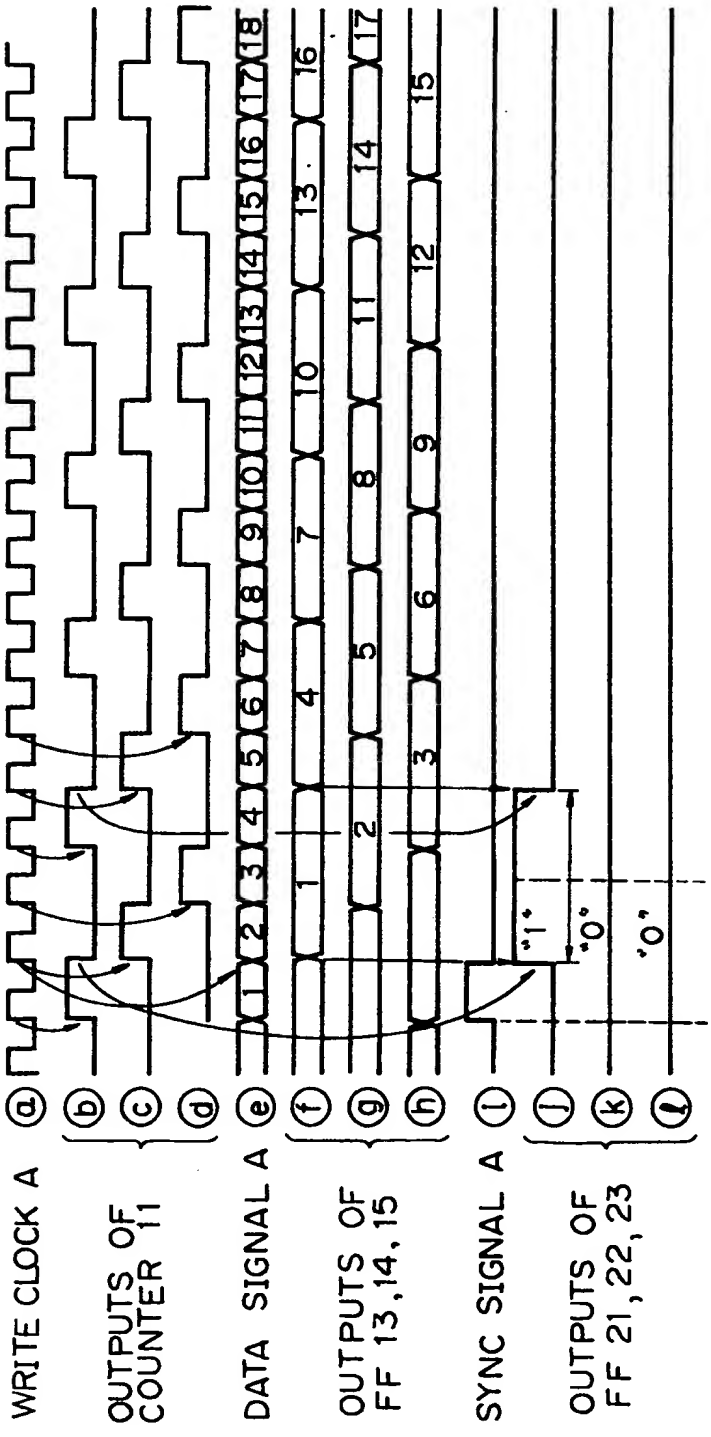

WRITE CLOCK A
OUTPUTS OF COUNTER 11
DATA SIGNAL A
OUTPUTS OF FF 13,14,15
SYNC SIGNAL A
OUTPUTS OF FF 21,22,23
"1"
"0"
"0"

Fig. 6B

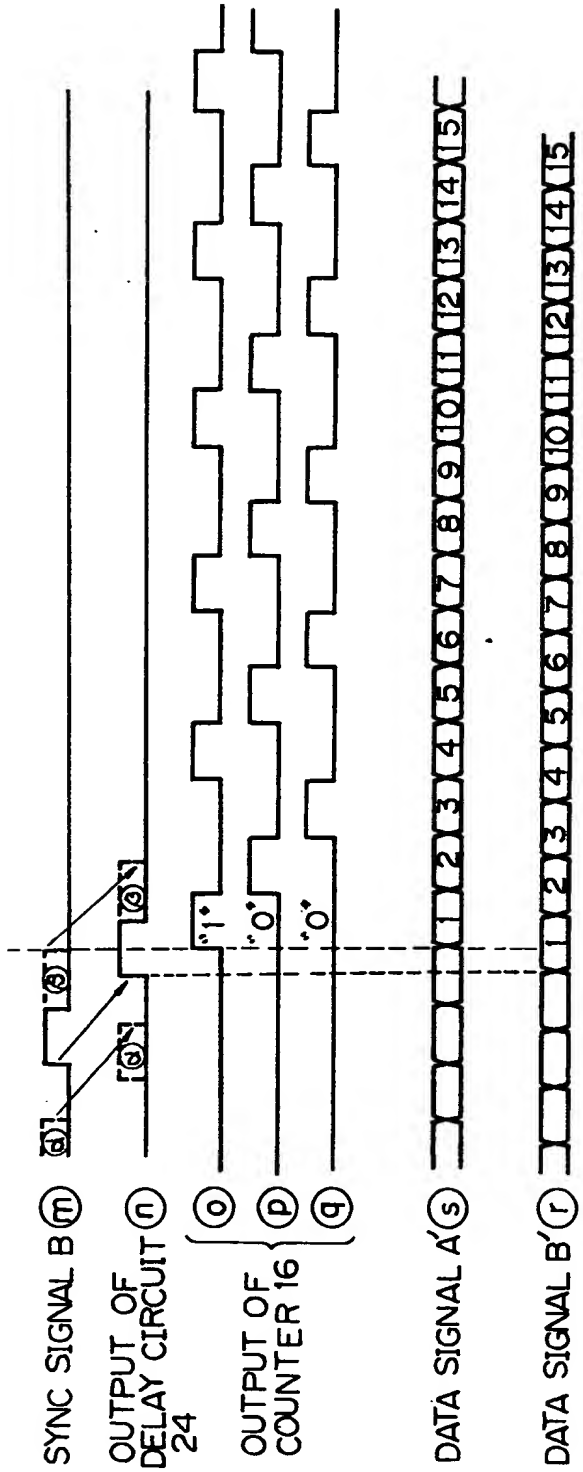
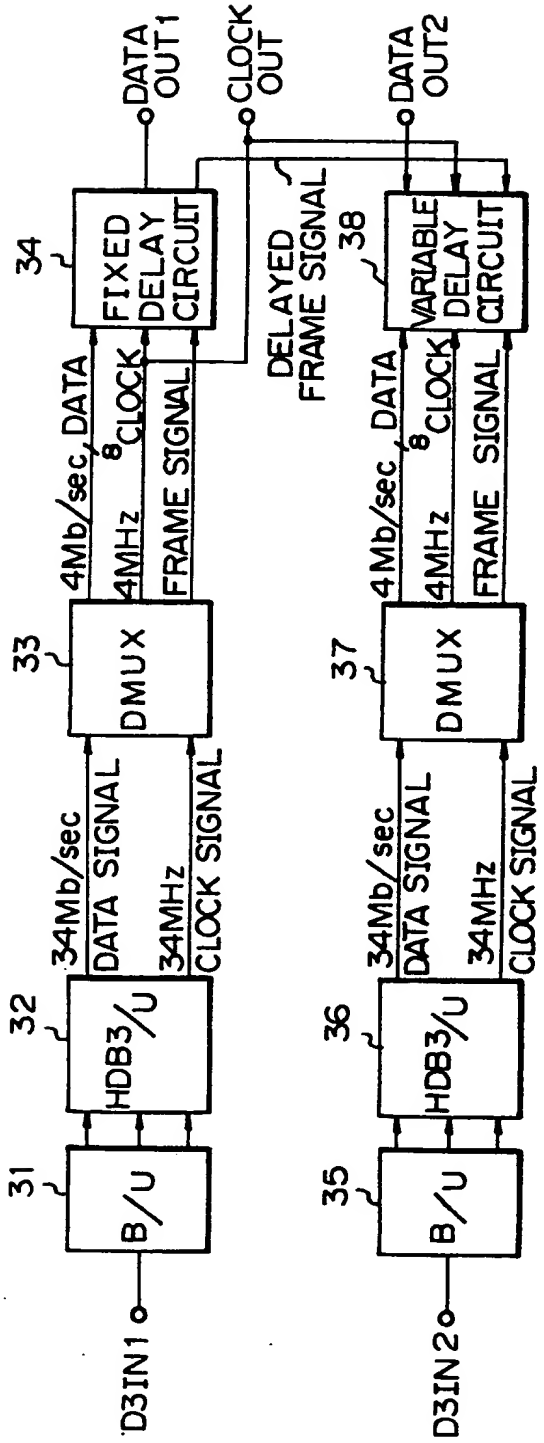

SYNC SIGNAL B (m)
OUTPUT OF DELAY CIRCUIT 24 (n)
OUTPUT OF COUNTER 16
(o)
(p)
(q)
"1"
"0"
"0"
DATA SIGNAL A' (s)
DATA SIGNAL B' (r)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Fig. 7


D3IN1
D3IN2
B/U
HDB3/U
DMUX
FIXED DELAY CIRCUIT
VARIABLE DELAY CIRCUIT
31
32
33
34
35
36
37
38
34Mb/sec DATA SIGNAL
34MHz CLOCK SIGNAL
4Mb/sec DATA
8 4MHz CLOCK
FRAME SIGNAL
DELAYED FRAME SIGNAL
DATA OUT1
CLOCK OUT
DATA OUT2